

<b>Notice of References Cited</b>	Application/Control No. 10/651,521	Applicant(s)/Patent Under Reexamination MAIN ET AL.	
	Examiner Jeremy S. Cerullo	Art Unit 2112	Page 1 of 1

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	U	Creating a PCI Express™ Interconnect - Ajay V. Bhatt, Technology and Research Labs, Intel Corporation - 2002
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.